

Notice of References Cited

Application/Control No.

10/711,472

Applicant(s)/Patent Under
Reexamination
CHEN ET AL.

Examiner

Russell Frejd

Art Unit

2128

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U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2004/0225459	11-2004	Krishnaswamy et al.	702/057
	B	US-			
*	C	US-2002/0188904	12-2002	Chen et al.	714/741
*	D	US-7,124,342	10-2006	Wang et al.	714/741
*	E	US-6,789,223	09-2004	Fetherson, R. Scott	714/738
*	F	US-6,678,645	01-2004	Rajsuman et al.	703/20
*	G	US-6,453,437	09-2002	Kapur et al.	714/741
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	ZARRINEH et al., K. System-on-chip testability using LSSD scan structures, IEEE Design & Test of Computers, Vol. 18, May-June 2001, pp. 83-97.
	V	ASTROM et al., P. Application of Software design patterns to DSP library design, Proceedings of the 14th International Symposium on Systems Synthesis, September 2001, pp. 239-43.
	W	ZORIAN et al., Testing embedded-core-based system chips, Computer, IEEE, Vol. 32, June 1999, pp. 52-60.
	X	GUPTA et al., R.K. Introducing core-based system design, IEEE Design & Test of Computers, Vol. 14, Oct.-Dec. 1997, pp. 15-25.

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
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	A	US-			
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	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	ARMSTRONG et al., J.R. VHDL Modeling and Model Testing for DSP Applications, IEEE Transactions on Industrial Electronics, Vol. 46, No. 1, February 1999, pp. 13-22.
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.